Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. – 11. (canceled)

12. (currently amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream;

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block; and

~~The display engine of claim 4 further comprises~~ a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream.

13. (currently amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream;

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block; and

~~The display engine of claim 4 further comprises~~ a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream.

14. (cancelled)

15. (currently amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block,

~~The display engine of claim 4,~~ wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling ratio, wherein the preferred video scaling ratio is based on the ratio between the video images in the first format and the output video image.

16. (currently amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block,

~~The display engine of claim 4,~~ wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred graphics scaling ratio, wherein the preferred graphics scaling ratio is based on the ratio between the graphics images in the second format and the output graphics image.

17. (cancelled)

18. (currently amended) A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream;

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block; and

~~The display engine of claim 4 further comprises~~ a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream.

19. – 23. (cancelled)

24. (currently amended) A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream,

~~The method of claim 20,~~ wherein scaling the video data further comprises removing the flicker from the scaled video stream.

25. (currently amended) A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream.

~~The method of claim 20,~~ wherein scaling the video data further comprises removing the flicker from the scaled graphics stream.

26. – 28.

29. (currently amended) A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream,

~~The method of claim 20,~~ wherein receiving the graphics data stream further comprises receiving the graphics data stream in a compressed format, wherein the graphics data stream is decompressed prior to scaling.

30. (cancelled)

31. (previously presented) A video graphics circuit comprising:

a plurality of memory blocks, wherein each of the plurality of memory blocks stores at least one of video data and graphics data;

a plurality of video scalers, wherein each of the plurality of video scalers is coupled to at least one of the plurality of memory blocks, wherein each video scaler of the plurality of video scalers independently scales at least a portion of the video data to produce a scaled video data stream of a plurality of scaled video data streams independent from the other scaled video data streams of the plurality of scaled video data streams;

a plurality of graphics scalers, wherein each of the plurality of graphics scalers is coupled to at least one of the plurality of memory blocks, wherein each graphics scaler of the plurality of graphics scalers independently scales at least a portion of the graphics data to produce a scaled graphics data stream of a plurality of scaled graphics data streams independent from the other scaled graphics data streams of the plurality of scaled graphics data streams; and

a plurality of merging blocks, wherein each of the merging blocks is operably coupled to at least one video scaler of the plurality of video scalers and at least one graphics scaler of the plurality of graphics scalers such that each of the merging blocks receives a plurality of scaled data streams, wherein each merging block combines received scaled data streams to produce a video graphics output stream of a plurality of video graphics streams.

32. (previously presented) The video graphics circuit of claim 31, wherein the plurality of video scalers, the plurality of graphics scalers, and the plurality of merging bocks are included in an integrated circuit.

33. (previously presented) The video graphics circuit of claim 32, wherein at least a portion of the plurality of memory blocks is included in the integrated circuit.

34. (previously presented) The video graphics circuit of claim 31 further comprises a plurality of controllers, wherein each of the plurality of controllers is operably coupled to at least one scaler of a combined set of scalers that includes the plurality of graphics scalers and the plurality of video scalers, wherein each of the plurality of controllers provides separate control information that controls independent scaling by scalers to which it is coupled.

35. (previously presented) The video graphics circuit of claim 34, wherein each of the plurality of controllers provides merging control information to one of the plurality of merging blocks, wherein the merging control information is used in combining the received scaled data stream by each merging block.

36. (currently amended) The video graphics circuit of claim 31, wherein each of the plurality of merging blocks perform alpha blend operations [[in]]to combine the received scaled data streams.

37. (currently amended) The video graphics circuit of claim 31, wherein the plurality of merging blocks ~~produce~~ produces the plurality of video graphics output streams in at least one of an analog display format and a digital display format.

38. (cancelled)